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| EXAMINER | |
|---|---|
| GUBIOTTI, MATTHEW P | |

| ART UNIT | PAPER NUMBER |
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| 2124 | |

DATE MAILED: 04/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/624,131 | Applicant(s) KAPUR ET AL. | |
|---|---|---|---|
| | Examiner Matthew Gubiotti | Art Unit 2124 | |

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-36* is/are rejected.

7)☒ Claim(s) *1 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Claim Objections*

2. Claim 1 is objected to because of the following informalities: The term "interconnecting" is misspelled in Line 15. Appropriate correction is required. It is noted that the Examiner has not performed a detailed review for spelling and grammatical errors in the specification, such a review by the Applicant is encouraged in response to this action.

### *Specification*

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9, 11, 12, and 15-17 recite the limitation "hardware model". There is insufficient antecedent basis for this

limitation in the claim. The claim has been further treated below, with the Examiner reading the limitation as "hardware description language model".

5. Claims 10, 11, 13, 16, 21 and 22 recites the limitation "software model". There is insufficient antecedent basis for this limitation in the claim. The claim has been further treated below, with the Examiner reading the limitation as "software language model".

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-11, 18-22 and 24-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Aleksic (U.S. Pat. No 5,995,735).

***Claim 1***

Aleksic teaches a method for designing a circuit substantially as claimed (col.3, li.53-59) comprising:

A central specification ("register specification source file") for an integrated circuit, designating a plurality of cores ("register layers") and interconnections between them (col.3, li.61 to col.4, li.11);

Establishing a set of software language models for the cores, each model implementing a an internal algorithm of one of the cores (col.3, li.61-66; fig.6B) and generating software language interconnection code ("connection templates"; col.5, li.55-62) for interconnecting the software language models to generate a software language model of the circuit ("behavioral model"; col.5, li.19-31; fig.1, ref.12);

Establishing a set of hardware description language models for the cores, each hardware description language model implementing an internal logic of one of the cores (col.3, li.61-66; fig.6D) and generating hardware description language interconnection code ("connection templates"; col.5, li.55-62) for interconnecting the hardware description language models to generate a hardware description language model of the circuit (col.4, li.24-32; fig.1, ref.10; fig.2, ref.38).

***Claim 2***

Aleksic further teaches the central specification designating a set of input and output tokens for each core ("register layer"); and a set of token fields for each interconnection (fig.6A; col.9, li.7-28).

***Claims 3-6***

Aleksic further teaches wherein generating the hardware description language core interconnection code comprises generating a set of port declarations (fig.6E, li.14-30), an interface port list (fig.6E, li.14-30), a set of data type definitions (fig.6A, col.2, li.20-40), and a set of bus definitions (fig.6A, col.3, li.19-26).

***Claim 7***

Aleksic further teaches wherein at least one of the token fields includes a field parameter with an associated value (fig.6A, col.2, li.30).

***Claims 8***

Aleksic further teaches generating a hardware description language declaration for each core (fig.6E, li.15-16).

***Claim 9***

Aleksic further teaches wherein the central specification defines core parameters (fig.6A; col.9, li.20-28) and generates the hardware description language model from a set of hardware

description language parameters declarations derived from a set of core parameters (col.3, li.66 to col.4, li.3; fig.6D&E).

***Claim 10***

Aleksic further teaches wherein the central specification defines a set of input and output tokens (fig.6A; col.9, li.7-28) and generates the software language model from the sets of tokens. Aleksic further teaches the specification enabling various components of the model to exchange data tokens through the use of communication pathways. (col.6, li.53-56; fig.3, ref.49).

***Claim 11***

Aleksic further teaches generating a test bench for comparing results from a software simulation of the circuit and a hardware simulation of a circuit (col.4, li.48-55, fig.1, refs.20,26&28).

***Claims 18 and 19***

Aleksic further teaches generating a synthesis restraint for limiting the fraction of a clock cycle used by an interface (fig.6D, col.2, li.8-18).

***Claims 20-22***

Aleksic further teaches instantiating a hardware sub-core model (fig.6D, col.1, li.18-33) in generating the hardware description language model and instantiating a software sub-core

model in generating the software language model (fig.6B, col.1, li.1-31).

***Claim 24***

This claim is rejected on the same reasons as set forth in rejecting claim 1 above.

***Claim 25***

This claim is rejected on the same reasons as set forth in rejecting claims 3-6 above.

***Claim 26***

This claim is rejected on the same reasons as set forth in rejecting claim 8 above.

***Claims 27 and 29***

These claims are rejected on the same reasons as set forth in rejecting claim 10 above.

***Claim 28***

This claim is rejected on the same reasons as set forth in rejecting claim 9 above.

***Claim 30***

This bulk of this claim is rejected for the same reasons set forth in rejecting claims 1 and 11 above. Aleksic further teaches generating a set of logic constraints from a specification (*See* col.9 li.20 to col.11, li.15; fig.6A). The definition and limitation of parameters as taught in the header

and body section of the central specification ("register specification source file") of Aleksic provides logic constraints on the behavior of the circuit.

***Claim 31***

This claim is rejected on the same reasons as set forth in rejecting claim 1 above.

***Claim 32***

This is the system claim representing the method described in claim 1. It rejected for the same reasons set forth above, with the system referenced as follows (fig.3; col.3, li.20-23).

***Claim 33-35***

These represent the medium claims representing the method described in claim 1. It rejected for the same reasons set forth above, with the medium referenced as follows (fig.4, ref.76; col.3, li.24-27; col.7, li.3-17).

***Claim 36***

This represents the apparatus claim representing the method described in claim 1. It rejected for the same reasons set forth above, with the apparatus referenced as follows (fig.3; col.3, li.20-23).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aleksic as applied to claim 1 above, and further in view of Gupte (U.S. Pat. No. 5,903,475).

***Claims 12-15***

Aleksic teaches a test bench for comparing results of software and hardware tests related to integrated circuit design (IC), but not expressly disclose the level of detail expressed in the claims. In the analogous art of IC design and verification testing, Gupta discloses:

a test bench comprising a bus driver for driving the hardware model (Claim 12; col.9, li.22-23; col.10, li.38-40), a software driver for driving the software model of the integrated circuit (Claim 13; col.9, li.10-13), a monitor module for comparing the results of the software and hardware simulations (Claim 14, col.9, li.39-41; fig.5, ref.368), and a bus receiver

module for requesting tokens from the hardware model (Claim 15, col.10, li.39-45);

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to combine the testing methodology of Gupte with the method Aleksic. The modification would have been obvious because one of ordinary skill in the art would have been motivated to simultaneously compare results from hardware and software simulations during various phases of IC circuit design to meet performance requirements and reduce design cycle time as taught by both Aleksic (col.3, li.1-6) and Gupte (col.1, li.53-59).

***Claims 16-17***

Gupte further discloses:

driving a hardware model with a simulation hardware input ("stand-alone simulation", col.2, li.7-16);

driving a software model with a simulation software input ("system simulation", col.2, li.7-16);

detecting the responses of the inputs ("outputs"; col.2, li.7-16);

comparing the results (col.2, li.13-16); and

wherein the driving of a software model and the comparison of result occurs at least in part concurrently with a simulation of a hardware model ("comparing the outputs…during system

simulation and stand-alone simulation outputs"; col.19, li.24-26).

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to combine the testing methodology of Gupte with the method Aleksic. The modification would have been obvious because one of ordinary skill in the art would have been motivated to simultaneously compare results from hardware and software simulations during various phases of IC circuit design to meet performance requirements and reduce design cycle time as taught by both Aleksic (col.3, li.1-6) and Gupte (col.1, li.53-59).

*Conclusion*

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Gubiotti whose telephone number is (703) 305-8285. The examiner can normally be reached on M-F, 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MPG
March 26, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100